2. (Amended) The device of claim 1 wherein the resistivity of said second layer is [higher] lower than that of said first layer.

3. (Amended) The device of claim 1 wherein the thickness of said first layer is [more] greater than that of said second layer.

4. (Amended) The device of claim 2 wherein the thickness of said first layer is [more] greater than that of said second layer.

A 1 (concluded)

5. (Amended) The device of claim 1 wherein said device has a given blocking voltage; and wherein the total thickness of said first and second layers is less than the thickness of a single [epitaxial] layer of epitaxial silicon designed to block the [same] given blocking voltage.

6. (Amended) The device of claim 2 wherein said device has a given blocking voltage; and wherein the total thickness of said first and second layers is less than the thickness of a single [epitaxial] layer of epitaxial silicon designed to block [the same] said given blocking voltage.

7. (Amended) The device of claim 3 wherein said device has a given blocking voltage; and wherein the total thickness of said first and second layers is less than the thickness of a single [epitaxial] layer of epitaxial silicon designed to block [the same] said given blocking voltage.

8. (Amended) The device of claim 4 wherein said device has a given blocking voltage; and wherein the total thickness of said first and second layers is less than the thickness of a single [epitaxial] layer of epitaxial silicon designed to block [the same] said given blocking voltage.

10. (Amended) A vertical conduction power MOSFET device having a reduced on-resistance; said device comprising a silicon substrate having a drain electrode on the bottom surface thereof, and [an epitaxially deposited] a layer of epitaxial silicon on the upper surface of said substrate and coextensive therewith; said [epitaxial deposited] layer having a graded concentration of one of the conductivity types from its top free surface to its bottom; an upper portion of said [epitaxial] layer extending from its free surface receiving a P-N junction which at least partly defines said power MOSFET and having an average impurity concentration which is more than the average concentration of the bottom portion of said [epitaxial] layer; said bottom portion of said [epitaxial] layer comprising more than 50% of the total thickness of said [epitaxial] layer.

11. (Amended) The device of claim 10 wherein said lower and upper portions of said [epitaxial] layer comprise respective separately [deposited] formed first and second layers of respective uniform concentration [or the upper portion of uniform doped epitaxial layer receives extra same type ion implantation and drive process].

12. (Amended) The device of claim 11 wherein said device having a given blocking voltage; and wherein the total thickness of said first and second layers is less than the thickness of a single [epitaxial] layer of epitaxial silicon designed to block the [same] given blocking voltage.

REMARKS

This application now contains claims 1 to 12, all but claim 9 of which are amended.

Applicant thanks the examiner for pointing out informalities in the claims (paragraphs 1, 3 and 4). The claims have been amended to correct the matters which were raised. The claims have also been amended to designate the epitaxially deposited layer (or layers) as a positive layer of distinct structure.